TSMC Launches OIP 3DFabric Alliance to Shape the Future of Semiconductor and System Innovations

The Expanded TSMC Open Innovation Platform Drives New Ecosystem Collaboration to Enable Next-Generation HPC and Mobile Applications

Hsinchu, Taiwan, R.O.C. – Oct. 27, 2022 – TSMC (TSE: 2330, NYSE: TSM) today announced the Open Innovation Platform® (OIP) 3DFabric Alliance at the 2022 Open Innovation Platform Ecosystem Forum. The new TSMC 3DFabric™ Alliance is TSMC's sixth OIP Alliance and the first of its kind in the semiconductor industry that joins forces with partners to accelerate 3D IC ecosystem innovation and readiness, with a full spectrum of best-in-class solutions and services for semiconductor design, memory modules, substrate technology, testing, manufacturing, and packaging. This alliance will help customers achieve speedy implementation of silicon and system-level innovations and enable next-generation HPC and mobile applications using TSMC's 3DFabric technologies, a comprehensive family of 3D silicon stacking and advanced packaging technologies.

"3D silicon stacking and advanced packaging technologies open the door to a new era of chip-level and system-level innovation, and also require extensive ecosystem collaboration to help designers navigate the best path through the myriad options and approaches available to them," said Dr. L.C. Lu, TSMC fellow and vice president of design and technology platform. "Through the collective leadership of TSMC and our ecosystem partners, our 3DFabric Alliance offers customers an easy and flexible way to unlocking the power of 3D IC in their designs, and we can't wait to see the innovations they can create with our 3DFabric technologies."

"As a pioneer in both chiplets and 3D silicon stacking, AMD is excited about the introduction of TSMC's 3DFabric Alliance and the vital role it will play in accelerating system-level innovation," said AMD senior vice president of technology & product engineering Mark Fuselier. "We've already seen the benefits of working with TSMC and its OIP partners on the world's first TSMC-SoIC™-based CPUs, and we're looking forward to collaborating even more closely to drive the development of a robust chiplet stacking ecosystem for future generations of energy-efficient, high-performance chips."

OIP 3DFabric Alliance

As the industry's most comprehensive and vibrant ecosystem, the TSMC OIP consists of six alliances: the EDA Alliance, IP Alliance, Design Center Alliance (DCA), Value Chain Alliance

(VCA), Cloud Alliance, and now, the 3DFabric Alliance. TSMC launched OIP in 2008 to help customers overcome the rising challenges of semiconductor design complexity by creating a new paradigm of collaboration, organizing development and optimization across TSMC's technologies, electronic design automation (EDA), IP, and design methodology.

Partners of the new 3DFabric Alliance have early access to TSMC's 3DFabric technologies, enabling them to develop and optimize their solutions in parallel with TSMC. This gives customers a head start on their product development with early availability of the highest-quality, readily-available solutions and services from **EDA** and **IP** to **DCA/VCA, Memory, OSAT** (Outsourced Semiconductor Assembly and Test), **Substrate,** and **Testing**.

"The Amazon Annapurna Labs team is responsible for building innovation in silicon for Amazon Web Services customers, and we have been collaborating with TSMC closely as we develop our AWS Trainium product using TSMC's advanced packaging technologies including CoWoS® and its support infrastructure from architecture definition, package design, and process validation, to successful production," said Nafea Bshara, Amazon Web Services vice president and distinguished engineer. "As a TSMC customer, we are pleased by the introduction of TSMC's OIP 3DFabric Alliance, which demonstrates TSMC's leadership and commitment to next-generation 3D IC design enablement."

New Collaboration with 3DFabric Alliance Partners

- **EDA** partners have early access to the TSMC 3DFabric technologies for EDA tool development and enhancement to offer optimized EDA tools and design flows to enable 3D IC designs more efficiently.
- **IP** partners develop 3D IC IPs compliant with die-to-die interface standards and TSMC 3DFabric technologies to provide a broad variety of highest-quality, proven IP solutions for customers.
- **DCA/VCA** partners gain early collaboration with mutual customers in 3DFabric technologies and roadmap alignment with TSMC that will improve their service capability for 3DFabric design, IP integration, and production.
- **Memory** partners have early technology engagement to define specs and early alignment on engineering and technical criteria with TSMC that will shorten time-to-market for future HBM generations to meet 3D IC design requirements.
- **OSAT** partners supporting TSMC's production quality and technical requirements collaborate with TSMC to fulfill customers' production demands with continuous improvements in all aspects of technology and production enablement and support.
- **Substrate** partners have early technology engagement and development with TSMC to meet future requirements of 3DFabric technologies that will improve substrate material

quality, reliability, and new substrate integration to speed up production of customers' 3D IC designs.

- **Testing** partners have early collaboration with TSMC to develop test and stress methodologies for TSMC's 3DFabric technologies, offering comprehensive coverage of reliability and quality requirements to help customers quickly launch their differentiated products.

"NVIDIA has been manufacturing with TSMC's CoWoS® technologies and supporting infrastructure for several generations of high-performance GPU products," said Joe Greco, senior vice president, advanced technology group, NVIDIA. "TSMC's new 3DFabric Alliance will extend the technology to a broader set of products and an enhanced level of integration."

TSMC 3Dblox™

To address the rising complexity of 3D IC design, TSMC introduced the TSMC 3Dblox™ standard to unify the design ecosystem with qualified EDA tools and flows for TSMC 3DFabric technology. The modularized TSMC 3Dblox standard is designed to model, in one format, the key physical stacking and the logical connectivity information in 3D IC designs. TSMC has worked with EDA partners in the 3DFabric alliance to enable 3Dblox for every aspect of 3D IC designs, including physical implementation, timing verification, physical verification, electro-migration IR drop (EMIR) analysis, thermal analysis, and more. TSMC 3Dblox is designed to maximize flexibility and ease of use, offering ultimate 3D IC design productivity.

TSMC 3DFabric Technologies

TSMC 3DFabric, a comprehensive family of 3D silicon stacking and advanced packaging technologies, further extends the Company's advanced semiconductor technology offerings to unleash system-level innovations. TSMC's 3DFabric consists of both frontend, 3D chip stacking or TSMC-SoIC™ (System on Integrated Chips), and backend technologies that include the CoWoS® and InFO family of packaging technologies, enabling better performance, power, form factor, and functionality to realize system-level integrations. In addition to CoWoS and InFO that have been in volume production, TSMC also started TSMC-SoIC silicon stacking manufacturing in 2022. TSMC now has the world's first fully automated fab for 3DFabric in Chunan, Taiwan that integrates advanced testing, TSMC-SoIC, and InFO operations together, offering the best flexibility for customers to optimize their packaging by leveraging better cycle time and quality control.

ENDS

Alliance Member Quotes:

Advantest

"Advantest has been actively working with TSMC in chip testing for many years," said **Juergen Serrer, executive vice president of Advantest's SoC business unit**. "We're excited about TSMC's new 3DFabric Alliance, and we look forward to collaborating on 3D-related chip testing such as power management, handling, design for test (DFT), and system-test at sort to fulfill customer demands."

Alchip

"As an experienced, mass production 2.5D ASIC provider, Alchip looks forward to joining the TSMC 3DFabric Alliance," said **Johnny Shen, president and CEO of Alchip Technologies.** "This new initiative solidifies TSMC's semiconductor leadership by providing strategic opportunities for leading-edge, high-performance ASIC companies to extend the most advanced packaging capabilities to innovative technology companies."

Alphawave

"Alphawave IP is very excited to be a founding partner in the TSMC 3DFabric Alliance as die-to-die interconnects are a very promising technology that we've been investing in for a long time," said **Tony Pialis, president and chief executive officer of Alphawave.** "TSMC is a long-time leader in building ecosystems that enable its customers to build the world's best semiconductor products and we look forward to working with TSMC in this new alliance to accelerate new technology and enable chiplet products to enter into the mainstream."

Amkor

"Amkor, a leading OSAT provider, welcomes the creation of TSMC's OIP 3DFabric Alliance as a catalyst for closer collaboration among multiple partners from design to advanced packaging, assembly, and test. OSATs are a critical extension of TSMC's manufacturing and enable optimization of IC performance, power, and area (PPA)," said **Kevin Engel, corporate vice president flipchip and wafer level business unit at Amkor**. "Amkor is honored to join this Alliance to support industry growth vectors, such as high-performance computing, artificial intelligence, networking, and wireless communications."

Ansys

"3D IC technology is triggering major changes in semiconductor design methods by blurring the distinction between chip design and system design," said **John Lee, vice president and general manager of the semiconductor, electronics, and optics business unit at Ansys**. "With strong market positions in both semiconductor signoff and system level simulation, Ansys is well

situated to collaborate with TSMC's 3DFabric Alliance in delivering proven solutions and open design platforms for 3D IC design to our mutual customers."

ARM

"Chiplets will be increasingly prevalent in the next generation of compute solutions, and Arm Neoverse platforms adopt 2.5D and 3D design to enable high core counts and heterogenous combinations with a diversity of accelerators, memory, and IO," said **Dermot O'Driscoll, vice president of product management, infrastructure line of business, Arm.** "Arm is excited to join the TSMC 3DFabric Alliance to enable our mutual customers to innovate faster, with increased compute and cache resources optimized for yield and cost, allowing for silicon upgrades and reuse."

ASE

"ASE is excited to be part of the TSMC 3DFabric Alliance, which will allow us to optimize our advanced packaging technologies together with other best-in-class partners within the 3D IC ecosystem," said **Mike Hung, senior vice president of central engineering, ASE Inc.** "The exponential growth of the high-performance computing (HPC) market is accelerating the role of heterogeneous integration. ASE has already built a robust technology portfolio to help customers achieve superior computing performance and better power efficiency. Joining this new Alliance will augment our capability to offer customers complete turnkey services and bring their products to market faster."

Cadence

"Over the years, Cadence has worked closely with TSMC on EDA and IP collaborations to enable customers to successfully leverage TSMC 3DFabric technologies," said **Dr. Chin-Chi Teng, senior vice president and general manager of the digital & signoff group at Cadence**. "Our latest collaboration with TSMC includes EDA innovations on TSMC 3Dblox standard and the certification of the Integrity 3D IC platform, our unified 3D IC planning, implementation, and analysis solution. On IP, we've delivered the 40Gbps/channel Ultralink D2D PHY IP and the 112G-XSR PHY IP, illustrating a strong roadmap for the Universal Chiplet Interconnect Express (UCIe) standard for connecting chiplets. By joining the new OIP 3DFabric Alliance, we're reinforcing our commitment to jointly advance design and analysis innovation across emerging multi-chiplet-based technologies for hyperscale computing, mobile, 5G, and AI applications."

GUC

"We are looking forward to participating in TSMC 3DFabric Alliance at a time when advanced packaging technologies have begun a design revolution for HPC, AI, and network processors. Adopting TSMC's 3DFabric technologies such as TSMC-SoIC allows much more efficient

connectivity for these designs," said **Dr. Sean Tai, president of GUC.** "As a long-standing TSMC OIP partner, GUC has successfully developed a platform to shorten design cycles and allow for low risk, high yield production of ASICs adopting TSMC 2.5D and 3D technologies."

IBIDEN

"The development of information and communication technology requires further integration and performance improvement of semiconductors," said **Mr. Koji Kawashima, director & senior executive officer at IBIDEN**. "IBIDEN welcomes TSMC's initiative to launch the 3DFabric Alliance to further develop 3D packaging technology and will contribute to product realization in cooperation with joint partners."

Micron

"Micron has been working closely with TSMC in previous and current High Bandwidth Memory (HBM) generations for CoWoS process compatibility and HBM interaction," said **Akshay Singh, vice president of advanced packaging technology development at Micron**. "Micron is excited to join TSMC's OIP 3DFabric Alliance and will help expand the scope with deeper collaboration in the delivery of solutions for future HBM generations to support customers' success in system product innovations."

Samsung Memory

"Samsung Memory has been in close collaboration with TSMC in previous and current HBM generations for CoWoS process compatibility and HBM interaction," said **Kyungsoo Ha, vice president of memory product planning group, Samsung Electronics**. "Samsung Memory joining TSMC's OIP 3DFabric Alliance will further expand the scope of work and delivery of solutions for future HBM generations to help customers unleash system-level innovations."

Siemens

"Siemens EDA has worked closely with TSMC for years to qualify more of our industry-leading tools and flows, as demand for sophisticated 3D IC design solutions has grown over time," said **Joe Sawicki, executive vice president of IC-EDA for Siemens Digital Industries Software**. "Today, that work has been formalized by Siemens extending its partnership with TSMC to now include participation in the foundry's new OIP 3DFabric Alliance. We look forward to continuing to deliver highly innovative new products and flows for our mutual customers to use in their design of 3D IC technology solutions."

Silicon Creations

"We recognize the importance of 3D stacking and advanced packaging technologies in enabling continued performance increases and cost management for leading integrated circuit products,"

said **Randy Caplan, principal/co-founder of Silicon Creations**. “As a leading supplier of clocking and interconnect solutions for TSMC’s leading process technologies, Silicon Creations is proud to join other top silicon IP providers as founding members of TSMC’s 3DFabric Alliance to provide robust IP solutions for the adaptive clocks demanded by stacked die.”

Siliconware Precision Industries

“As a leading provider of assembly and test, we are consistently collaborating with TSMC and are excited to join the new 3DFabric Alliance to enable system innovation and cutting-edge technology,” said **Dr. Yu-Po Wang, vice president of corporate R & D, Siliconware Precision Industries Co., Ltd**. “By utilizing top notch 3DFabric technologies, the flexible silicon stacking and modularity enable the best value for the product and customer.”

SK hynix

“SK hynix has been working closely with TSMC in previous and current HBM generations for CoWoS process compatibility and HBM interaction,” said **Dr. Kangwook Lee, senior vice president, head of PKG development at SK hynix**. “By joining the new 3DFabric Alliance, SK hynix is engaging in even deeper collaboration with TSMC to deliver solutions for future HBM generations and enable system product innovations.”

Synopsys

“Through the new 3DFabric Alliance, Synopsys and TSMC are accelerating multi-die system design for cost-effective integration, optimized performance and energy efficiency,” said **Sassine Ghazi, president and chief operating officer at Synopsys**. “We bring unified EDA and system design solutions and an IP portfolio that is the broadest in the industry. And together with TSMC’s 3DFabric technologies, we’re enabling our mutual customers to efficiently handle all aspects of multi-die design and heterogeneous integration to support advanced packaging for complex, compute-intensive applications.”

Teradyne

“Teradyne is excited to be a founding member of TSMC’s 3DFabric Alliance,” said **Regan Mills, vice president of SoC marketing at Teradyne**. “Early collaboration with TSMC and other alliance members will ensure the development of new, comprehensive test methodologies, accelerating readiness of the ecosystem and enabling faster time to market all while meeting or exceeding stringent quality objectives.”

Unimicron

“With a goal of being the global leading substrate supplier, Unimicron is dedicated to quality-adhered production and customer-oriented service,” said **Unimicron Chairman T.J. Tseng. “**It's

our great pleasure to join TSMC's new 3DFabric Alliance. As a member of the Alliance, Unimicron has been given the opportunity to contribute to the innovation of packaging technologies, and to develop and optimize advanced solutions in parallel with other semiconductor and tech leaders. Together with TSMC, we will provide our mutual customers with high-quality solutions in a timely manner."

About TSMC Open Innovation Platform (OIP)

TSMC launched the Open Innovation Platform in 2008 to reduce design barriers and promote the speedy implementation of innovation in the semiconductor design community by bringing together the creative thinking of customers and partners. TSMC's Open Innovation Platform (OIP) brings together the creative thinking of customers and partners under the common goal of shortening design time, time-to-volume, time-to-market and ultimately, time-to-revenue. The TSMC OIP features the most comprehensive design ecosystem alliance programs covering industry-leading EDA, library, IPs, Cloud, and design service partners. TSMC has worked closely with these ecosystem partners ever since the Company was established and continues to expand its libraries and silicon IP portfolio to more than 55,000 IP titles and provides more than 43,000 technology files and over 2,900 process design kits, from 0.5-micron to 3-nanometer, to customers.

About TSMC

TSMC pioneered the pure-play foundry business model when it was founded in 1987 and has been the world's leading dedicated semiconductor foundry ever since. The Company supports a thriving ecosystem of global customers and partners with the industry's leading process technologies and portfolio of design enablement solutions to unleash innovation for the global semiconductor industry. With global operations spanning Asia, Europe, and North America, TSMC serves as a committed corporate citizen around the world.

TSMC deployed 291 distinct process technologies and manufactured 12,302 products for 535 customers in 2021 by providing broadest range of advanced, specialty, and advanced packaging technology services. TSMC is the first foundry to provide 5-nanometer production capabilities, the most advanced semiconductor process technology available in the world. The Company is headquartered in Hsinchu, Taiwan. For more information, please visit https://www.tsmc.com.

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