



TSMC Announces Breakthrough Set to Redefine the Future of 3D IC

New 3Dblox 2.0 and 3DFabric Alliance Achievements Detailed at 2023 OIP Ecosystem Forum

SANTA CLARA, CA, September 27, 2023 – TSMC (TSE: 2330, NYSE: TSM) today announced the new 3Dblox 2.0 open standard and major achievements of its Open Innovation Platform® (OIP) 3DFabric Alliance at the TSMC 2023 OIP Ecosystem Forum. The 3Dblox 2.0 features early 3D IC design capability that aims to significantly boost design efficiency, while the 3DFabric Alliance continues to drive memory, substrate, testing, manufacturing, and packaging integration. TSMC continues to push the envelope of 3D IC innovation, making its comprehensive 3D silicon stacking and advanced packaging technologies more accessible to every customer.

“As the industry shifted toward embracing 3D IC and system-level innovation, the need for industry-wide collaboration has become even more essential than it was when we launched OIP 15 years ago,” said Dr. L.C. Lu, TSMC fellow and vice president of Design and Technology Platform. “As our sustained collaboration with OIP ecosystem partners continues to flourish, we’re enabling customers to harness TSMC’s leading process and 3DFabric technologies to reach an entirely new level of performance and power efficiency for the next-generation artificial intelligence (AI), high-performance computing (HPC), and mobile applications.”

“We have been working closely with TSMC on advanced 3D packaging technology which enables AMD’s next-generation MI300 accelerators to offer industry-leading performance, memory footprint, and bandwidth for AI and supercomputing workloads,” said Mark Fuselier, senior vice president of Technology and Product Engineering at AMD. “Together with their 3DFabric Alliance partners, TSMC has developed a broad 3Dblox ecosystem that has helped AMD accelerate time-to-market for our 3D chiplet product portfolio.”

3Dblox 2.0

Introduced last year, the 3Dblox open standard aims to modularize and streamline 3D IC design solutions for the semiconductor industry. With contribution from the largest ecosystem of companies, 3Dblox has emerged as a critical design enabler of future 3D IC advancement.

The new 3Dblox 2.0, launched today, enables 3D architecture exploration with an innovative early design solution for power and thermal feasibility studies. The designer can now, for the first time in the industry, put together power domain specifications and 3D physical constructs in a holistic environment and simulate power and thermal for the whole 3D system. 3Dblox 2.0 also supports chiplet design reuse features such as chiplet mirroring to further improve design



productivity.

3Dblox 2.0 has won support from key EDA partners to develop design solutions that fully support all TSMC 3DFabric offerings. Those comprehensive design solutions provide designers with key insights to make early design decisions, accelerating design turnaround time from architecture to final implementation.

TSMC also launched the 3Dblox Committee, organized as an independent standard group, with the goal to create an industry-wide specification that enables system design with chiplets from any vendors. Working with key members including Ansys, Cadence, Siemens, and Synopsys, the committee has ten technical groups of different subjects and proposes enhancements to the specs and maintain the interoperability of EDA tools. Designers can now download the latest 3Dblox specifications from the 3dblox.org website and find more information about 3Dblox and its tool implementation by EDA partners.

3DFabric Alliance Achievements

As the first of its kind in the semiconductor industry, TSMC's 3DFabric Alliance has grown tremendously over the past year, working toward the goal of providing customers with a full spectrum of proven solutions and services for semiconductor design, memory modules, substrate technology, testing, manufacturing, and packaging. Now the Company has 21 3DFabric Alliance partners across the industry to collaborate and innovate with.

Memory Collaboration: Generative AI and large language model-related applications require more SRAM memory and higher DRAM memory bandwidth. To meet this requirement, TSMC has worked closely with its key memory partners including Micron, Samsung Memory, and SK hynix to drive rapid growth on HBM3 and HBM3e to advance generative AI systems by delivering more memory capacity.

Substrate Collaboration: TSMC has worked successfully with substrate partners IBIDEN and UMTC to define a Substrate Design Tech file to facilitate substrate auto-routing for significant efficiency and productivity gains. The Company initiated a three-way collaboration with substrate and EDA partners with the goal to deliver 10x productivity gains from automatic substrate routing. The collaboration also includes design for manufacturing (DFM) enhancement rules to reduce stress hotspot in substrate design.

Testing Collaboration: TSMC is collaborating with automatic test equipment (ATE) partners Advantest and Teradyne to solve a variety of 3D test challenges to reduce any yield loss and improve power delivery efficiency for chiplet testing. To demonstrate high-speed test access for



3D stack testing through functional interface, TSMC is working with Synopsys and ATE partners on a silicon demonstrator to achieve the goal of 10x testing productivity boost. The Company is also working with all design-for-test (DFT) EDA partners to ensure effective and efficient interface testing.

About TSMC Open Innovation Platform (OIP)

TSMC launched the Open Innovation Platform in 2008 to reduce design barriers and promote the speedy implementation of innovation in the semiconductor design community by bringing together the creative thinking of customers and partners with the common goal of shortening design time, time-to-volume, time-to-market and ultimately, time-to-revenue. TSMC OIP features the most comprehensive design ecosystem alliance programs covering industry-leading EDA, library, IPs, Cloud, and design service partners. TSMC has worked closely with these ecosystem partners ever since the Company was established and continues to expand its libraries and silicon IP portfolio to more than 70,000 IP titles and provides more than 46,000 technology files and over 3,300 process design kits, from 0.5-micron to 2-nanometer, to customers.

About TSMC

TSMC pioneered the pure-play foundry business model when it was founded in 1987 and has been the world's leading dedicated semiconductor foundry ever since. The Company supports a thriving ecosystem of global customers and partners with the industry's leading process technologies and portfolio of design enablement solutions to unleash innovation for the global semiconductor industry. With global operations spanning Asia, Europe, and North America, TSMC serves as a committed corporate citizen around the world.

TSMC deployed 288 distinct process technologies and manufactured 12,698 products for 532 customers in 2022 by providing broadest range of advanced, specialty, and advanced packaging technology services. The Company is headquartered in Hsinchu, Taiwan. For more information, please visit <https://www.tsmc.com>.

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TSMC Spokesperson:

Wendell Huang
Vice President and CFO
Tel: 886-3-505-5901

Media Contacts:

Nina Kao
Head of Public Relations
Tel: 886-3-563-6688 ext.7125036
Mobile: 886-988-239-163
E-Mail: nina_kao@tsmc.com

Tiffany Yang
Public Relations Manager
Tel: 1-408-382-7934
E-Mail: tiffany@tsmc.com