TSMC Showcases New Technology Developments at 2023 Technology Symposium

Debuts Enhanced N3P Process, HPC-Focused N3X Process, N3AE Auto Early Program, and Updates 2nm and TSMC 3DFabric™ Progress

SANTA CLARA, CA, Apr. 26, 2023 – TSMC (TWSE: 2330, NYSE: TSM) today showcased its latest technology developments at its 2023 North America Technology Symposium, including progress in 2nm technology and new members of its industry-leading 3nm technology family, offering a range of processes tuned to meet diverse customer demands. These include N3P, an enhanced 3nm process for better power, performance and density, N3X, a process tailored for high performance computing (HPC) applications, and N3AE, enabling early start of automotive applications on the most advanced silicon technology.

With more than 1,600 customers and partners registered to attend, the North America Technology Symposium in Santa Clara, California is the first of the TSMC's Technology Symposiums around the world in the coming months. The North America symposium also features an Innovation Zone spotlighting the exciting technologies of 18 emerging start-up customers.

"Our customers never stop finding new ways to harness the power of silicon to create innovations that shall amaze the world for a better future," said Dr. C.C. Wei, CEO of TSMC. "In the same spirit, TSMC never stands still, and we keep enhancing and advancing our process technologies with more performance, power efficiency, and functionality so their pipeline of innovation can continue flowing for many years to come."

Key technologies highlighted at the Symposium include:

Broader 3nm Portfolio: N3P, N3X, and N3AE – With 3nm technology now in volume production with the N3 process and the enhanced N3E version on the way in 2023, TSMC is adding new variants to the roadmap to suit customers' diverse needs.

- N3P, scheduled to enter production in the second half of 2024, offers an additional boost to N3E with 5% more speed at the same leakage, 5-10% power reduction at the same speed, and 1.04X more chip density.
- N3X, which prioritizes performance and maximum clock frequencies for HPC applications, provides 5% more speed versus N3P at drive voltage of 1.2V, with the same improved chip density as N3P, and will enter volume production in 2025.
- N3AE, or "Auto Early", available in 2023, offers automotive process design kits (PDKs) based on N3E, and allows customers to launch designs on the 3nm node for automotive applications, leading to the fully automotive-qualified N3A process in 2025.

2nm Technology Making Solid Progress – Development of TSMC's 2nm technology employing nanosheet transistors is making solid progress in both yield and device performance, and is on track for production in 2025. It will provide up to 15% speed improvement over N3E at the same power, and up to 30% power reduction at the same speed, and greater than 1.15X chip density.

Pushing the Limits of CMOS RF Technology with N4PRF – Beyond the N6RF technology announced in 2021, TSMC is developing N4PRF, the industry's most advanced CMOS radio frequency technology for digital-intensive RF applications such as WiFi 7 RF system-on-chip. N4PRF will support 1.77X greater logic density and 45% less logic power at the same speed compared with N6RF.

TSMC 3DFabric™ Advanced Packaging and Silicon Stacking – major new developments in TSMC's 3DFabric system integration technologies include:

- Advanced Packaging – To support the demands of HPC applications to fit more processors and memory in a single package, TSMC is developing Chip on Wafer on Substrate (CoWoS) solution with up to 6 times reticle-size (~5,000mm^2) RDL interposer, capable of accommodating 12 stacks of HBM memory.
- 3D Chip Stacking – TSMC announced SoIC-P, microbump versions of its System on Integrated Chips (SoIC) solutions providing a cost-effective way for 3D chip stacking. SoIC-P complements TSMC's existing bumpless solutions for high-performance computing (HPC) applications, which are now known as SoIC-X.
- Design Support – TSMC introduced 3Dblox™ 1.5, the newest version of its open standard design language to lower the barriers to 3D IC design. 3Dblox™ 1.5 adds automated bump synthesis, helping designers deal with the complexities of large dies with thousands of bumps and potentially reducing design times by months.

About TSMC

TSMC pioneered the pure-play foundry business model when it was founded in 1987, and has been the world's leading dedicated semiconductor foundry ever since. The Company supports a thriving ecosystem of global customers and partners with the industry's leading process technologies and portfolio of design enablement solutions to unleash innovation for the global semiconductor industry. With global operations spanning Asia, Europe, and North America, TSMC serves as a committed corporate citizen around the world.

TSMC deployed 288 distinct process technologies, and manufactured 12,698 products for 532 customers in 2022 by providing broadest range of advanced, specialty and advanced packaging technology services. The Company is headquartered in Hsinchu, Taiwan. For more information please visit https://www.tsmc.com.

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