TSMC Research Highlighted at 2019 Symposia on VLSI Technology & Circuits

Hsinchu, Taiwan, R.O.C., June 6, 2019—TSMC today announced that papers on its advanced research into emerging memory, two-dimensional materials, and system integration technologies have been featured at the 2019 Symposia on VLSI Technology & Circuits, a premier conference in the field of microelectronics.

The VLSI Symposia, which will be held from June 9-14 in Kyoto, Japan, invited TSMC to deliver a paper on the state of research in embedded Magnetoresistive Random-Access Memory (eMRAM), and further highlighted three TSMC papers for addressing the theme of the 2019 conference, "Pushing the Limits of Semiconductors for a United and Connected World".

The papers showcase TSMC's technology leadership on all fronts – from innovative materials for transistors at the leading edge of advanced logic, to emerging high-performance embedded memory in our specialty technology portfolio, to system integration solutions offering our customers a unique cost/performance advantage.

"It is a great source of pride to TSMC that the VLSI Symposia not only highlighted our papers, but also invited us to present on our research." said Dr. H.-S. Philip Wong, TSMC's Vice President of Research and Development/Corporate Research. "These papers come from distinguished veteran researchers as well as promising young engineers. With our strong commitment to technology leadership, I am confident that TSMC will keep providing the technologies that unleash our customers' innovations for many years to come."

Invited Paper

TSMC was invited by the Symposia to deliver the paper **"Recent Progress and Next Directions for Embedded MRAM Technology"** addressing eMRAM, a nonvolatile memory with potential to replace conventional embedded flash, which is beginning to hit the limits of its scaling. This paper describes results for a 22nm eMRAM that is solder-reflow capable, meaning it is able to endure the high temperatures of soldering in the packaging process without losing data pre-stored in the memory during the wafer manufacturing process. Compared to 28nm embedded flash, it requires fewer additional mask layers, and delivers significant improvement in both write speed and endurance. This solder-reflow capable eMRAM is optimal for applications where retention of pre-stored data is critical, such as wearables and Internet of Things (IoT) devices. At the same time, the paper also shows that where solder-reflow capability is not required, enhanced eMRAM performance with lower write power consumption and faster read

time make it a viable, dense working RAM, which is also nonvolatile. Applications such as low-power consumption machine learning inference processors could benefit from these characteristics.

Highlighted Papers

One of the major challenges to transistor scaling at 3nm and beyond is that the channel allowing electrons to flow through a transistor must not only be shorter, but thinner as well to ensure good switching behavior. This has led to a search for so-called "two-dimensional" channel materials. TSMC's paper **"First Demonstration of 40nm Channel Length Top-Gate WS_2 pFET Using Channel Area-Selective CVD Growth Directly on SiO_x/Si Substrate"** demonstrates the potential for high-volume production using a promising 2D material, tungsten disulphide (WS_2). It describes a short-channel transistor with WS_2 channel made using the well-established semiconductor manufacturing process of chemical vapor deposition (CVD) directly on a silicon substrate. CVD offers a much simpler method of volume production than the conventional process of making a thin film of WS_2, which would require the material to be first deposited on a sapphire substrate, then removed and placed on a silicon wafer. The research shines additional light on the way forward for volume production of future generations of transistors.

TSMC's other two highlighted papers also address scaling, but at the level of an entire system rather than the individual transistor. Both offer a path to a system made up of "chiplets." Rather than the "system-on-chip" (SoC) approach combining every component of a system on a single die, chiplets split functions into small separate dies that can be made with different process technologies, offering both flexibility and cost savings. In addition, smaller dies inherently enjoy better yields than large dies. However, to achieve performance comparable to a SoC, chiplets must be able to communicate with each other through dense, high-speed, high-bandwidth connections.

TSMC's paper **"A 7nm 4GHz Arm® -core-based CoWoS® Chiplet Design for High-Performance Computing"** details a dual 7nm chiplet system in TSMC's Chip on Wafer on Substrate (CoWoS®) advanced packaging solution. Each chiplet features an Arm® core performing at 4GHz for high-performance computing applications. The paper also validates an on-die mesh bus, also operating at 4GHz, connecting the Arm core in each chiplet to its memory cache. In turn, the two chiplets connect with each other through TSMC's unique Low-voltage-In-Package-INterCONnect (LIPINCON™), reaching data rates of 8 gigabits per second per pin (Gb/s/pin) with good power efficiency, versus performance ranging from 2 to 5.3 Gb/s/pin for comparable interconnect solutions demonstrated in recent papers.

Finally, TSMC showcased its true 3D integration technology with the paper **"3D Multi-chip Integration with System on Integrated Chips (SoIC)"**. The SoIC solution enables known good dies of different sizes, process technologies, and materials to be directly stacked together. Compared to typical 3DIC solutions with micro-bumps, TSMC's SoIC delivers higher bump density and speed, while consuming much less power, the paper found. What's more, SoIC is a "front-end" integration solution connecting two or more dies before they are packaged. Therefore, a SoIC stack can be further integrated with other SoIC or chips in one of TSMC's "back-end" advanced packaging technologies such as InFO or CoWoS, offering a powerful "3D-by-3D" system-level solution.

In addition to the highlighted research above, TSMC also contributed to a paper by Qualcomm Inc., **"7nm Mobile SoC and 5G Platform Technology and Design Co-Development for PPA and Manufacturability",** reporting on Qualcomm's Snapdragon™ SDM855 mobile system-on-chip and world's first commercial 5G platform using 7nm FinFET technologies.

For media information on the 2019 Symposia on VLSI Technology and Circuits, including descriptions of highlighted papers, please visit http://vlsisymposium.org/press-kit/ .

About TSMC

TSMC pioneered the pure-play foundry business model when it was founded in 1987 and has been the world's largest dedicated semiconductor foundry ever since. The Company supports a thriving ecosystem of global customers and partners with the industry's leading process technology and portfolio of design enablement solutions to unleash innovation for the global semiconductor industry.

TSMC serves its customers with annual capacity of 12 million 12-inch equivalent wafers in 2019 from fabs in Taiwan, the United States, and China, and provides the broadest range of technologies from 0.5 micron plus all the way to foundry's most advanced processes, which is 7-nanometer today. TSMC is the first foundry to provide 7-nanometer production capabilities and is headquartered in Hsinchu, Taiwan. For more information about TSMC please visit http://www.tsmc.com.

# # #

TSMC Spokesperson:
Ms. Lora Ho
Senior Vice President and CFO
Tel: 886-3-566-4602

TSMC Acting Spokesperson:
Dr. Elizabeth Sun
Senior Director
Corporate Communications Division
Tel: 886-3-568-2085
Mobile: 886-988-937999
E-Mail: elizabeth_sun@tsmc.com

For Further Information:
Michael Kramer
Project Manager
PR Department
Tel: 886-3-5636688
Ext. 7125031
Mobile: 886-988-931-352
E-Mail: pdkramer@tsmc.com